

DUAL JK FLIP-FLOP WITH RESET; NEGATIVE-EDGE TRIGGER

FEATURES

- Output capability: standard
- I_{CC} category: flip-flops

GENERAL DESCRIPTION

The 74HC/HCT73 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT73 are dual negative-edge triggered JK-type flip-flops featuring individual J, K, clock (\overline{nCP}) and reset (\overline{nR}) inputs; also complementary Q and \overline{Q} outputs.

The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation.

The reset (\overline{nR}) is an asynchronous active LOW input. When LOW, it overrides the clock and data inputs, forcing the Q output LOW and the \overline{Q} output HIGH.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay \overline{nCP} to \overline{nQ} \overline{nCP} to \overline{nQ} \overline{nR} to \overline{nQ} , \overline{nQ}	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	16 16 15	15 18 15	ns ns ns
f_{max}	maximum clock frequency		77	79	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	30	30	pF

$GND = 0 \text{ V}$; $T_{amb} = 25^\circ\text{C}$; $t_r = t_f = 6 \text{ ns}$

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz
 f_o = output frequency in MHz
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
 C_L = output load capacitance in pF
 V_{CC} = supply voltage in V

2. For HC the condition is $V_I = GND$ to V_{CC}
For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 \text{ V}$

PACKAGE OUTLINES

14-lead DIL; plastic (SOT27)

14-lead mini pack; plastic (SO14; SOT108A)

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 5	$1\overline{CP}$, $2\overline{CP}$	clock input (HIGH-to-LOW, edge-triggered)
2, 6	$1\overline{R}$, $2\overline{R}$	asynchronous reset inputs (active LOW)
4	V_{CC}	positive supply voltage
11	GND	ground (0 V)
12, 9	$1Q$, $2Q$	true flip-flop outputs
13, 8	$1\overline{Q}$, $2\overline{Q}$	complement flip-flop outputs
14, 7, 3, 10	$1J$, $2J$, $1K$, $2K$	synchronous inputs; flip-flops 1 and 2

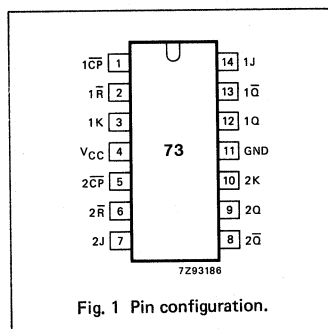


Fig. 1 Pin configuration.

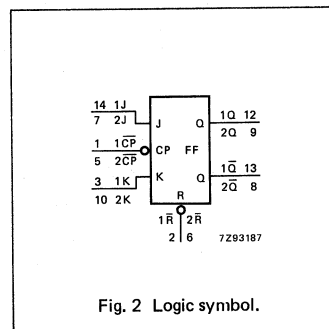


Fig. 2 Logic symbol.

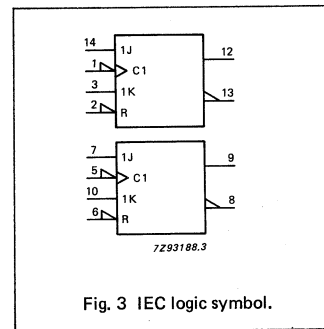
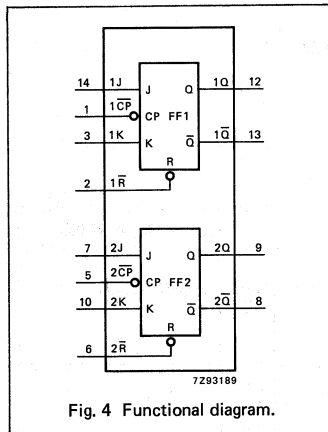


Fig. 3 IEC logic symbol.

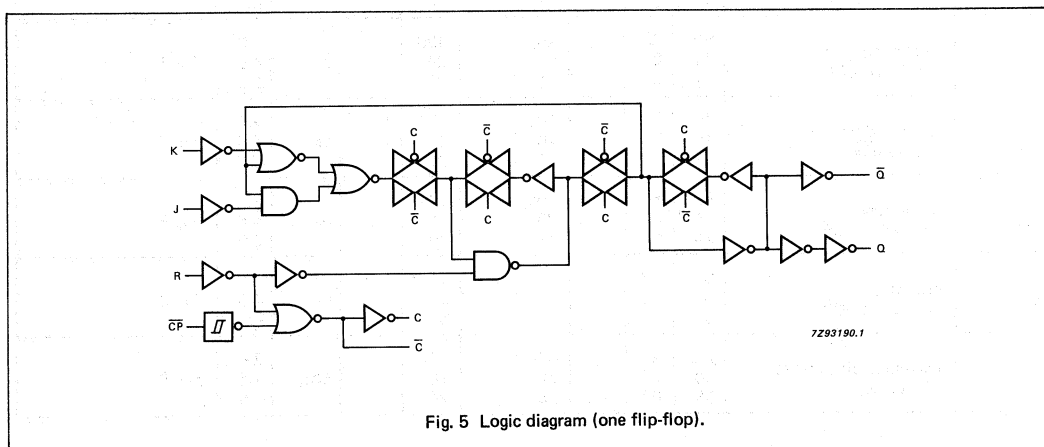
74HC/HCT73
flip-flops



FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	\overline{nR}	\overline{nCP}	J	K	Q	\overline{Q}
asynchronous reset	L	X	X	X	L	H
toggle	H	\downarrow	h	h	\overline{q}	q
load "0" (reset)	H	\downarrow	l	h	L	H
load "1" (set)	H	\downarrow	h	l	H	L
hold "no change"	H	\downarrow	l	l	q	\overline{q}

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW CP transition
X = don't care
 \downarrow = HIGH-to-LOW CP transition



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

 I_{CC} category: flip-flops

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS	
		74HC									V _{CC} V	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay nCP to nQ		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6	
t _{PHL} / t _{PLH}	propagation delay nCP to nQ̄		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6	
t _{PHL} / t _{PLH}	propagation delay nR to nQ, nQ̄		50 18 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 7	
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6	
t _W	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6	
t _W	reset pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7	
t _{rem}	removal time nR to nCP̄	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7	
t _{su}	set-up time nJ, nK to nCP̄	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6	
t _h	hold time nJ, nK to nCP̄	3 3 3	-8 -3 -2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 6	
f _{max}	maximum clock pulse frequency	6.0 30 35	23 70 83		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6	

74HC/HCT73
flip-flops

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I_{CC} category: flip-flops

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nK	0.60
nR	0.65
nCP, nJ	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74 HCT								V _{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay nCP to nQ		18	38		48		57	ns	4.5	Fig. 6
t _{PHL} / t _{PLH}	propagation delay nCP to nQ		21	36		45		54	ns	4.5	Fig. 6
t _{PHL} / t _{PLH}	propagation delay nR to nQ, nQ		20	34		43		51	ns	4.5	Fig. 7
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t _W	clock pulse width HIGH or LOW	16	8		20		24		ns	4.5	Fig. 6
t _W	reset pulse width HIGH or LOW	18	9		23		27		ns	4.5	Fig. 7
t _{rem}	removal time nR to nCP	14	8		18		21		ns	4.5	Fig. 7
t _{su}	set-up time nJ, nK to nCP	12	6		15		18		ns	4.5	Fig. 6
t _h	hold time nJ, nK to nCP	3	−2		3		3		ns	4.5	Fig. 6
f _{max}	maximum clock pulse frequency	30	72		24		20		MHz	4.5	Fig. 6

AC WAVEFORMS

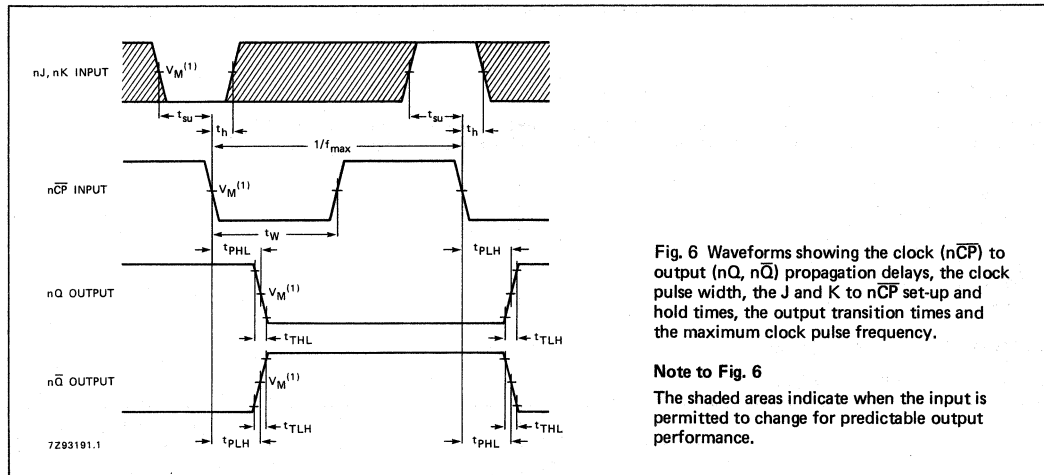


Fig. 6 Waveforms showing the clock (\overline{nCP}) to output (nQ , \overline{nQ}) propagation delays, the clock pulse width, the J and K to \overline{nCP} set-up and hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

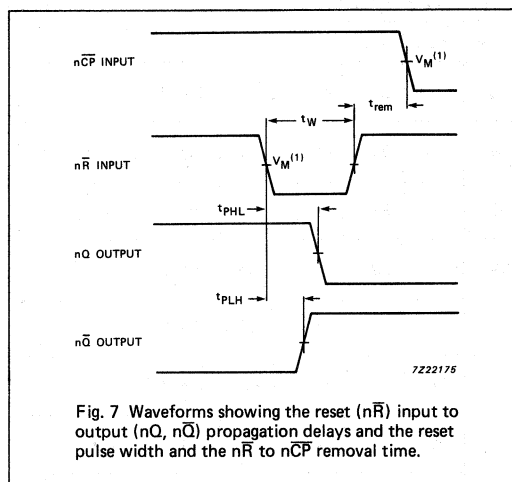


Fig. 7 Waveforms showing the reset (\overline{nR}) input to output (nQ , \overline{nQ}) propagation delays and the reset pulse width and the \overline{nR} to \overline{nCP} removal time.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.