

## QUAD D-TYPE FLIP-FLOP WITH RESET; POSITIVE-EDGE TRIGGER

## FEATURES

- Four edge-triggered D flip-flops
- Output capability: standard
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT175 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT175 have four edge-triggered, D-type flip-flops with individual D inputs and both Q and  $\bar{Q}$  outputs.

The common clock (CP) and master reset ( $\overline{MR}$ ) inputs load and reset (clear) all flip-flops simultaneously.

The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output ( $Q_n$ ) of the flip-flop.

All  $Q_n$  outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the  $\overline{MR}$  input.

The device is useful for applications where both the true and complement outputs are required and the clock and master reset are common to all storage elements.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub>	propagation delay CP to $Q_n$ , $\bar{Q}_n$ MR to $Q_n$	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	17 15	16 19	ns ns
			17 15	16 16	ns ns
t <sub>PLH</sub>	propagation delay CP to $Q_n$ , $\bar{Q}_n$ MR to $Q_n$		17 15	16 16	ns ns
f <sub>max</sub>	maximum clock frequency		83	54	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per flip-flop	notes 1 and 2	32	34	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in  $\mu$ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>

For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

## PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).

16-lead mini-pack; plastic (SO16; SOT109A).

## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	master reset input (active LOW)
2, 7, 10, 15	Q <sub>0</sub> to Q <sub>3</sub>	flip-flop outputs
3, 6, 11, 14	$\bar{Q}_0$ to $\bar{Q}_3$	complementary flip-flop outputs
4, 5, 12, 13	D <sub>0</sub> to D <sub>3</sub>	data inputs
8	GND	ground (0 V)
9	CP	clock input (LOW-to-HIGH, edge-triggered)
16	V <sub>CC</sub>	positive supply voltage

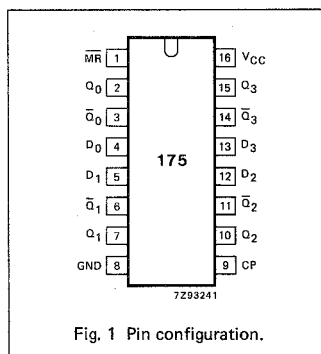


Fig. 1 Pin configuration.

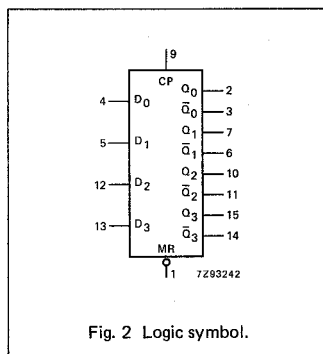


Fig. 2 Logic symbol.

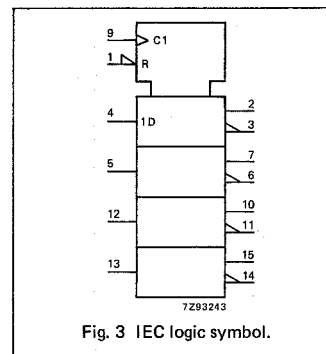
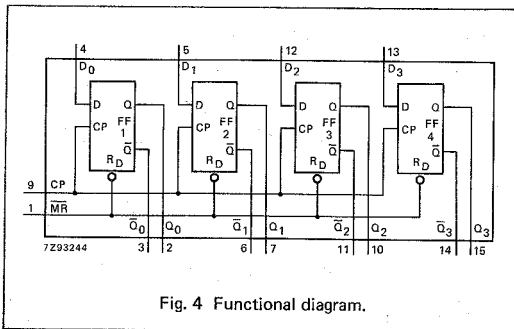


Fig. 3 IEC logic symbol.

74HC/HCT175

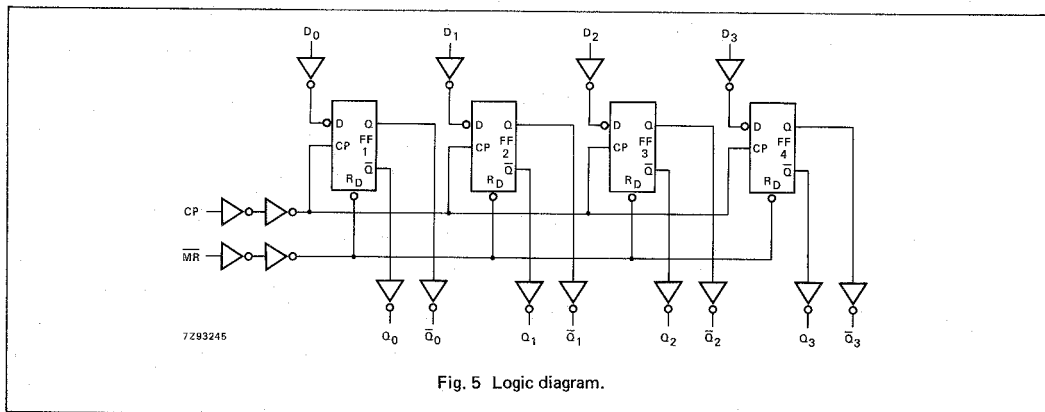
MSI



FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS	
	$\overline{MR}$	CP	$D_n$	$Q_n$	$\overline{Q}_n$
reset (clear)	L	X	X	L	H
load "1"	H	$\uparrow$	h	H	L
load "0"	H	$\uparrow$	l	L	H

H = HIGH voltage level  
h = HIGH voltage level one set-up time prior to the  
LOW-to-HIGH CP transition  
L = LOW voltage level  
l = LOW voltage level one set-up time prior to the  
LOW-to-HIGH CP transition  
 $\uparrow$  = LOW-to-HIGH CP transition  
X = don't care



**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

 $I_{CC}$  category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HC									V <sub>CC</sub> V	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub> , Q <sub>n</sub>		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay MR to Q <sub>n</sub> , Q <sub>n</sub>		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6	
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6	
t <sub>W</sub>	master reset pulse width LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8	
t <sub>rem</sub>	removal time MR to CP	5 5 5	-33 -12 -10		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8	
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	80 16 14	3 1 1		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7	
t <sub>h</sub>	hold time CP to D <sub>n</sub>	25 5 4	2 0 0		30 6 5		40 8 7		ns	2.0 4.5 6.0	Fig. 7	
f <sub>max</sub>	maximum clock pulse frequency	6.0 30 35	25 75 89		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6	

**74HC/HCT175****MSI****DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

$I_{CC}$  category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
MR	1.00
CP	0.60
$D_n$	0.40

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HCT								V <sub>CC</sub> V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub> , $\bar{Q}_n$		19	33		41		50	ns	4.5	Fig. 6
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		22	38		48		57	ns	4.5	Fig. 8
t <sub>PLH</sub>	propagation delay MR to $\bar{Q}_n$		19	35		44		53	ns	4.5	Fig. 8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	20	12		25		30		ns	4.5	Fig. 6
t <sub>W</sub>	master reset pulse width LOW	20	11		25		30		ns	4.5	Fig. 8
t <sub>rem</sub>	removal time MR to CP	5	−10		5		5		ns	4.5	Fig. 8
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	16	5		20		24		ns	4.5	Fig. 7
t <sub>h</sub>	hold time CP to D <sub>n</sub>	5	0		5		5		ns	4.5	Fig. 7
f <sub>max</sub>	maximum clock pulse frequency	25	49		20		17		MHz	4.5	Fig. 6

## AC WAVEFORMS

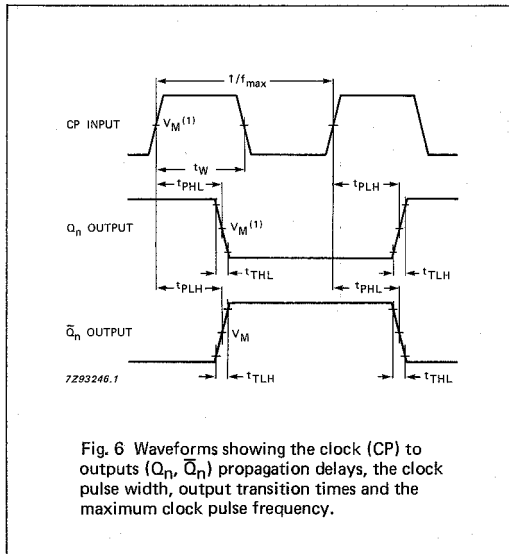


Fig. 6 Waveforms showing the clock (CP) to outputs ( $Q_n$ ,  $\bar{Q}_n$ ) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

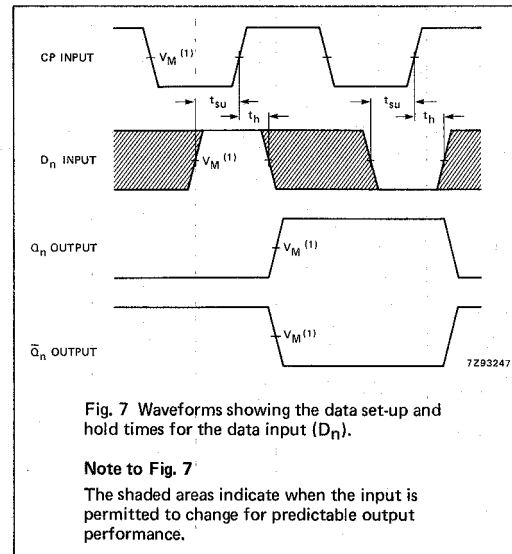


Fig. 7 Waveforms showing the data set-up and hold times for the data input ( $D_n$ ).

## Note to Fig. 7

The shaded areas indicate when the input is permitted to change for predictable output performance.

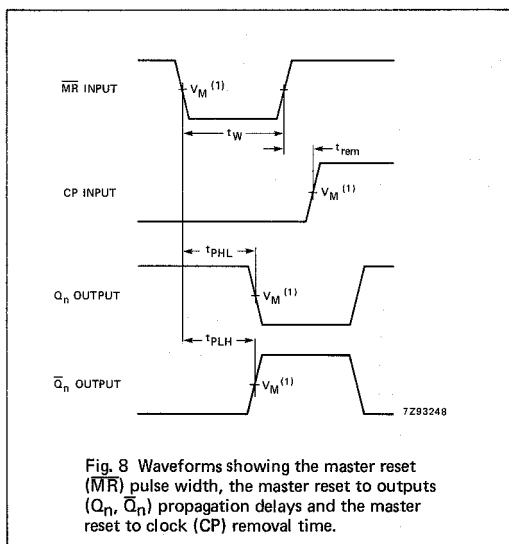


Fig. 8 Waveforms showing the master reset ( $\bar{MR}$ ) pulse width, the master reset to outputs ( $Q_n$ ,  $\bar{Q}_n$ ) propagation delays and the master reset to clock (CP) removal time.

## Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

