

MM54HCT193/MM74HCT193 Synchronous Binary Up/Down Counters

General Description

These high speed synchronous counters utilize advanced silicon-gate CMOS technology to achieve the high noise immunity and low power consumption of CMOS technology, along with the speeds of low power Schottky TTL. The MM54HCT193/MM74HCT193 is a binary counter having two separate clock inputs, an UP COUNT input and a DOWN COUNT input. All outputs of the flip-flops are simultaneously triggered on the low-to-high transition of either clock while the other input is held high. The direction of counting is determined by which input is clocked.

This device has TTL compatible inputs. It can drive 15 LS-TTL loads.

This counter may be preset by entering the desired data on the DATA A, DATA B, DATA C, and DATA D inputs. When the LOAD input is taken low, the data is loaded independently of either clock input. This feature allows the counter to be used as a divide-by-n counter by modifying the count length with the preset inputs.

In addition, the HCT193 can also be cleared. This is accomplished by inputting a high on the CLEAR input. All 4 internal stages are set to a low level independently of either COUNT input.

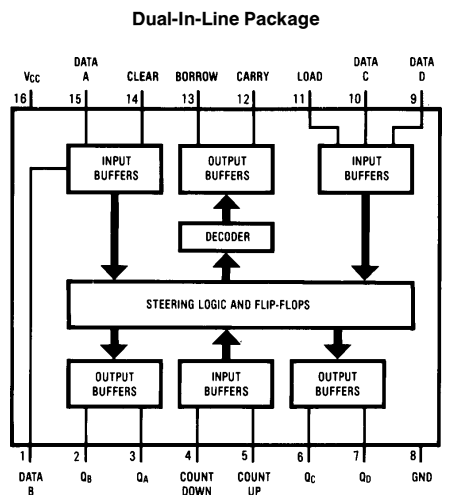
Both a BORROW and CARRY output are provided to enable cascading of both up and down counting functions. The BORROW output produces a negative-going pulse when the counter underflows and the CARRY outputs a pulse when the counter overflows. The counter can be cascaded by connecting the CARRY and BORROW outputs of one device to the COUNT UP and COUNT DOWN inputs, respectively, of the next device.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Low quiescent supply current: 80 μA maximum (74HCT Series)
- Low input current: 1 μA maximum
- TTL compatible inputs

Connection Diagram



Order Number MM54HCT193 or MM74HCT193

Truth Table

| Count | | Clear | Load | Function |
|-------|------|-------|------|------------|
| Up | Down | | | |
| ↑ | H | L | H | Count Up |
| H | ↑ | L | H | Count Down |
| X | X | H | X | Clear |
| X | X | L | L | Load |

H = high level

L = low level

↑ = transition from low-to-high

X = don't care

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|--------------------------|
| Supply Voltage (V_{CC}) | −0.5V to +7.0V |
| DC Input Voltage (V_{IN}) | −1.5V to V_{CC} + 1.5V |
| DC Output Voltage (V_{OUT}) | −0.5V to V_{CC} + 0.5V |
| Clamp Diode Current (I_{IK} , I_{OK}) | ±20 mA |
| DC Output Current, per Pin (I_{OUT}) | ±25 mA |
| DC V_{CC} or GND Current, per Pin (I_{CC}) | ±50 mA |
| Storage Temperature Range (T_{STG}) | −65°C to +150°C |
| Power Dissipation (P_D) | |
| (Note 3) | 600 mW |
| S.O. Package only | 500 mW |
| Lead Temperature (T_L) | |
| (Soldering, 10 seconds) | 260°C |

Operating Conditions

| | Min | Max | Units |
|---|-----|----------|-------|
| Supply Voltage (V_{CC}) | 4.5 | 5.5 | V |
| DC Input or Output Voltage (V_{IN} , V_{OUT}) | 0 | V_{CC} | V |
| Operating Temp. Range (T_A) | | | |
| MM74HCT | −40 | +85 | °C |
| MM54HCT | −55 | +125 | °C |
| Input Rise or Fall Times (t_r , t_f) | | 500 | ns |

DC Electrical Characteristics $V_{CC} = 5V \pm 10\%$ unless otherwise specified

| Symbol | Parameter | Conditions | T _A = 25°C | | 74HCT | 54HCT | Units |
|-----------------|-----------------------------------|--|-----------------------|-----------------------|-----------------------|-----------------------|-------|
| | | | Typ | Guaranteed Limits | | | |
| V _{IH} | Minimum High Level Input Voltage | | | 2.0 | 2.0 | 2.0 | V |
| V _{IL} | Maximum Low Level Input Voltage | | | 0.8 | 0.8 | 0.8 | V |
| V _{OH} | Minimum High Level Output Voltage | V _{IN} = V _{IH} or V _{IL} | | | | | |
| | | I _{OUT} = 20 μA | V _{CC} | V _{CC} − 0.1 | V _{CC} − 0.1 | V _{CC} − 0.1 | |
| | | I _{OUT} = 4.0 mA, V _{CC} = 4.5V | 4.2 | 3.98 | 3.84 | 3.7 | V |
| | | I _{OUT} = 4.8 mA, V _{CC} = 5.5V | 5.2 | 4.98 | 4.84 | 4.7 | V |
| V _{OL} | Maximum Low Level Voltage | V _{IN} = V _{IH} or V _{IL} | | | | | |
| | | I _{OUT} = 20 μA | 0 | 0.1 | 0.1 | 0.1 | V |
| | | I _{OUT} = 4.0 mA, V _{CC} = 4.5V | 0.2 | 0.26 | 0.33 | 0.4 | V |
| | | I _{OUT} = 4.8 mA, V _{CC} = 5.5V | 0.2 | 0.26 | 0.33 | 0.4 | V |
| I _{IN} | Maximum Input Current | V _{IN} = V _{CC} or GND, V _{IH} or V _{IL} | | ± 0.1 | ± 1.0 | ± 1.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current | V _{IN} = V _{CC} or GND I _{OUT} = 0 μA | | 8.0 | 80 | 160 | μA |
| | | V _{IN} = 2.4V or 0.5V (Note 4) | | 1.0 | 1.2 | 1.3 | mA |

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic “N” package: −12 mW/°C from 65°C to 85°C; ceramic “J” package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.

AC Electrical Characteristics

(Note 6) $V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 15\text{ pF}$, $t_r = t_f = 6\text{ ns}$ (unless otherwise specified)

| Symbol | Parameter | From (Input) | To (Output) | Conditions | Typ | Guaranteed Limit | Units |
|----------------|--------------------------------|-------------------|----------------|------------|-----|------------------|-------|
| f_{MAX} | Maximum Clock Frequency | | | | 35 | | MHz |
| $t_{PLH, PHL}$ | Maximum Propagation Delay Time | Load | QA, QB, QC, QD | | 26 | | ns |
| $t_{PLH, PHL}$ | Maximum Propagation Delay Time | Data A, B, C, D, | QA, QB, QC, QD | | 25 | | ns |
| $t_{PLH, PHL}$ | Maximum Propagation Delay Time | Count-Up or -Down | QA, QB, QC, QD | | 26 | | ns |
| $t_{PLH, PHL}$ | Maximum Propagation Delay Time | Count-Up | Carry | | 22 | | ns |
| $t_{PLH, PHL}$ | Maximum Propagation Delay Time | Count-Dn | Borrow | | 22 | | ns |
| $t_{PLH, PHL}$ | Maximum Propagation Delay Time | Clear | QA, QB, QC, QD | | 25 | | ns |

AC Electrical Characteristics (Note 6)

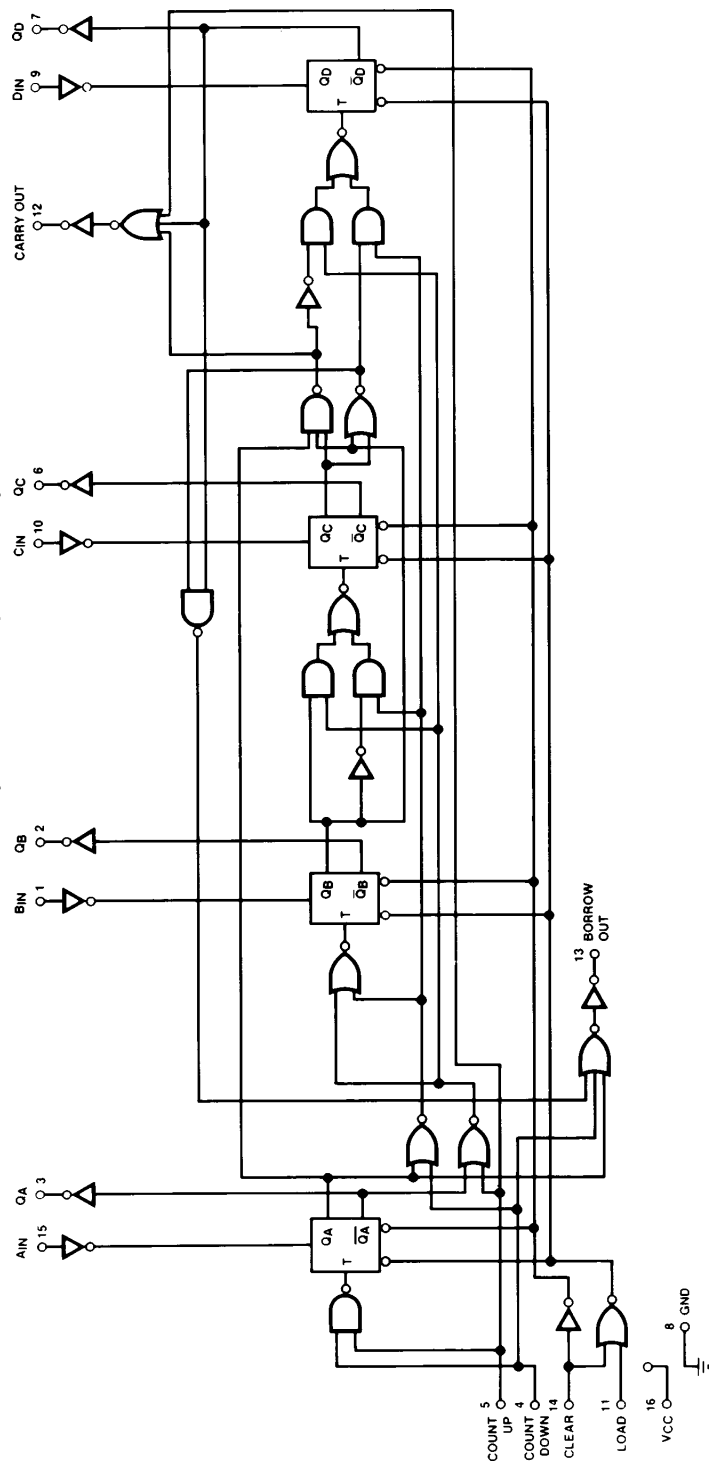
$V_{CC} = 5V$, $\pm 10\%$, $C_L = 50\text{ pF}$ (unless otherwise specified)

| Symbol | Parameter | From (Input) | To (Output) | T = 25°C | T = 25°C | 74HC T = −40° to 85°C | 54HC T = −55° to 125°C | Units |
|-----------------------|--|-------------------|----------------|----------|-------------------|--------------------------|---------------------------|-------|
| | | | | Typ | Guaranteed Limits | | | |
| f _{MAX} | Maximum Clock Frequency | | | 32 | 20 | 16 | 13 | MHz |
| t _{PLH, PHL} | Maximum Propagation Delay Time | Load | QA, QB, QC, QD | 29 | 44 | 55 | 66 | ns |
| t _{PLH, PHL} | Maximum Propagation Delay Time | Data A | QA, QB, QC, QD | 28 | 40 | 50 | 60 | ns |
| t _{PLH, PHL} | Maximum Propagation Delay Time | Count-Up or -Down | QA, QB QC, QD | 30 | 43 | 54 | 65 | ns |
| t _{PLH, PHL} | Maximum Propagation Delay Time | Count-Up | Carry | 25 | 30 | 38 | 45 | ns |
| t _{PLH, PHL} | Maximum Propagation Delay Time | Count-Down | Borrow | 25 | 30 | 38 | 45 | ns |
| t _{PLH, PHL} | Maximum Propagation Delay Time | Clear | QA, QB QC, QD | 28 | 35 | 44 | 53 | ns |
| t _W | Minimum Clock Pulse Width | | | 16 | 25 | 31 | 38 | ns |
| t _S | Minimum Setup Time Data before Load-LH | | | | 20 | 25 | 30 | ns |
| t _H | Minimum Hold Time Data after Load-LH | | | −3 | 5 | 6 | 8 | ns |
| t _{REM} | Minimum Removal Time Load to Count | | | −2 | 5 | 6 | 8 | ns |
| t _{REM} | Minimum Removal Time Clear to Count | | | 2 | 5 | 6 | 8 | ns |
| t _W | Minimum Load Pulse Width | | | 18 | 20 | 25 | 30 | ns |
| t _W | Minimum Clear Pulse Width | | | 8 | 20 | 25 | 30 | ns |
| t _{TLH, THL} | Output Rise or Fall Time | | | 10 | 15 | 19 | 22 | ns |
| C _{PD} | Power Dissipation Capacitance | | | 40 | | | | pF |
| C _{IN} | Maximum Input Capacitance | | | 5 | 10 | 10 | 10 | pF |

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

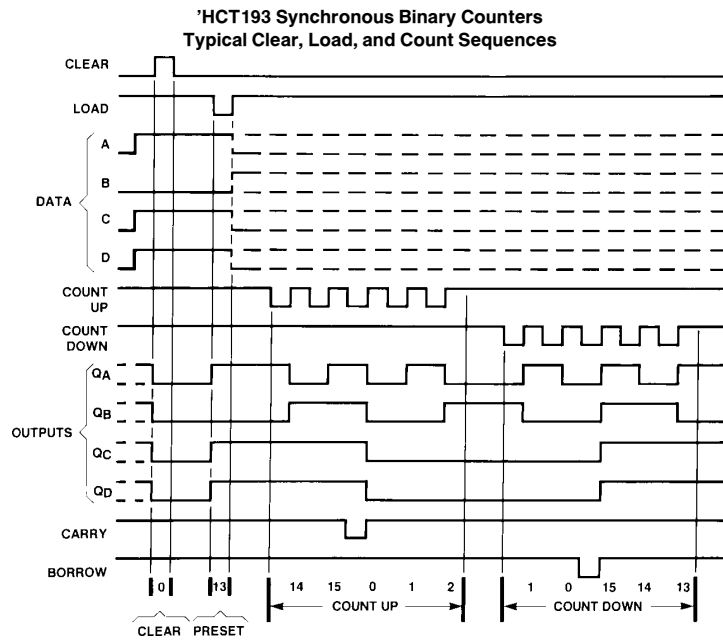
Note 6: Refer to Section 1 for Typical MM54/74HCT AC Switchforms and Test Circuits.

MM54HCT193/MM74HCT193 Synchronous 4-Bit Up/Down Binary Counter



TL/F/5742-2

Logic Waveforms



TL/F/5742-3

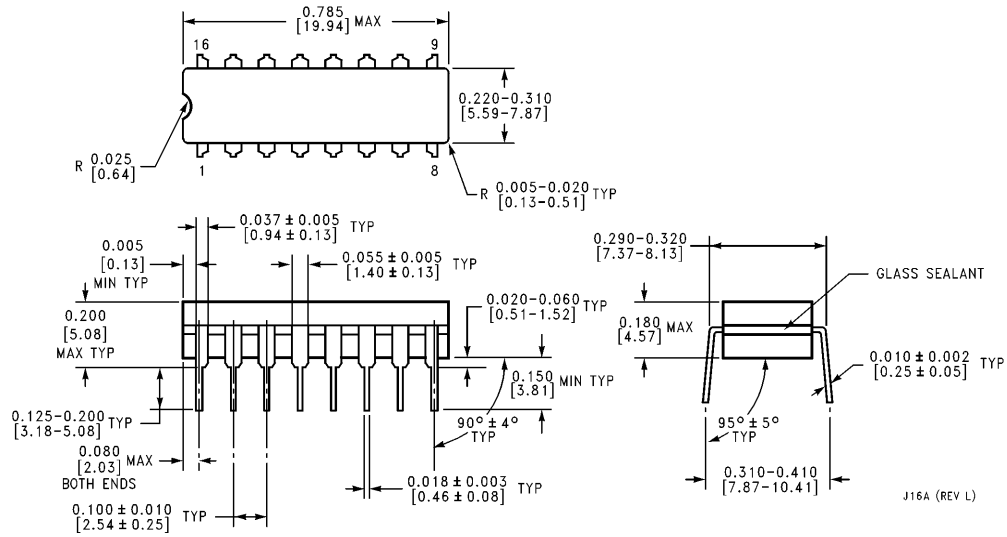
Sequence:

- (1) Clear outputs to zero.
- (2) Load (preset) to binary thirteen
- (3) Count up to fourteen, fifteen, carry, zero, one, and two.
- (4) Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

Note A: Clear overrides load data, and count inputs.

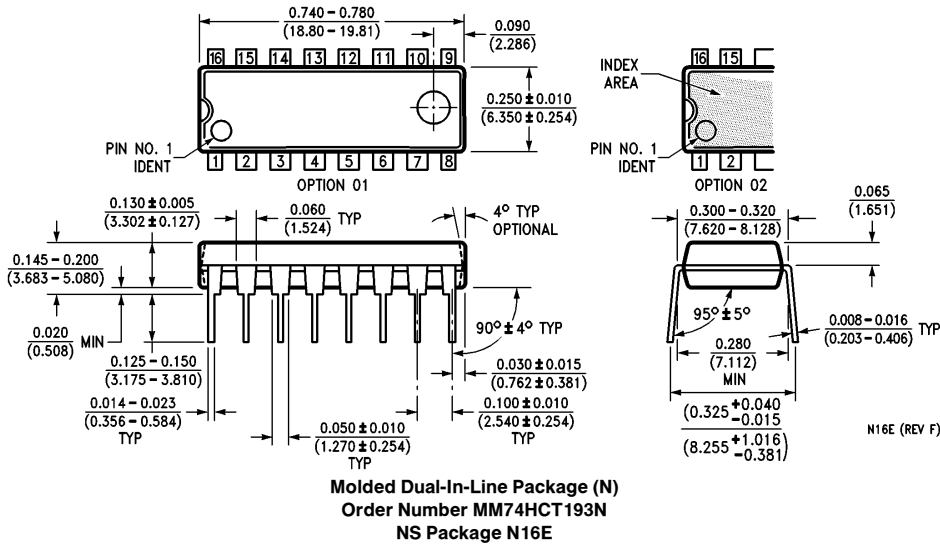
Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number MM54HCT193J or MM74HCT193J
NS Package J16A

Physical Dimensions inches (millimeters) (Continued)



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National Semiconductor Corporation
 1111 West Bardin Road
 Arlington, TX 76017
 Tel: 1(800) 272-9959
 Fax: 1(800) 737-7018

National Semiconductor Europe
 Fax: (+49) 0-180-530 85 86
 Email: cnjwge@tevm2.nsc.com
 Deutsch Tel: (+49) 0-180-530 85 85
 English Tel: (+49) 0-180-532 78 32
 Français Tel: (+49) 0-180-532 93 58
 Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
 13th Floor, Straight Block,
 Ocean Centre, 5 Canton Rd.
 Tsimshatsui, Kowloon
 Hong Kong
 Tel: (852) 2737-1600
 Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
 Tel: 81-043-299-2309
 Fax: 81-043-299-2408

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