

## 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

### FEATURES

- Shift-left and shift-right capability
- Synchronous parallel and serial data transfer
- Easily expanded for both serial and parallel operation
- Asynchronous master reset
- Hold ("do nothing") mode
- Output capability: standard
- $I_{CC}$  category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT194 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The functional characteristics of the 74HC/HCT194 4-bit bidirectional universal shift registers are indicated in the logic diagram and function table. The registers are fully synchronous.

The "194" design has special features which increase the range of application. The synchronous operation of the device is determined by the mode select inputs ( $S_0, S_1$ ). As shown in the mode select table, data can be entered and shifted from left to right ( $Q_0 \rightarrow Q_1 \rightarrow Q_2$ , etc.) or, right to left:

( $Q_3 \rightarrow Q_2 \rightarrow Q_1$ , etc.) or parallel data can be entered, loading all 4 bits of the register simultaneously. When both  $S_0$  and  $S_1$  are LOW, existing data is retained in a hold ("do nothing") mode. The first and last stages provide D-type serial data inputs ( $D_{SR}, D_{SL}$ ) to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

Mode select and data inputs are edge-triggered, responding only to the LOW-to-HIGH transition of the clock (CP). Therefore, the only timing restriction is that the mode control and selected data

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay CP to $Q_n$	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	14	15	ns
$t_{PHL}$	$\overline{MR}$ to $Q_n$		11	15	ns
$f_{max}$	maximum clock frequency		102	77	MHz
$C_i$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per package	notes 1 and 2	40	40	pF

GND = 0 V;  $T_{amb} = 25^\circ\text{C}$ ;  $t_r = t_f = 6 \text{ ns}$

### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz  
 $f_o$  = output frequency in MHz  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs  
 $C_L$  = output load capacitance in pF  
 $V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5 \text{ V}$

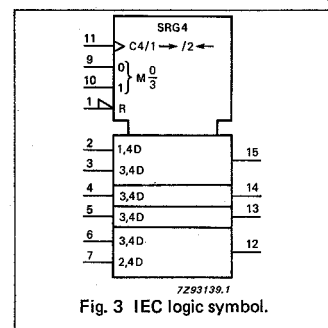
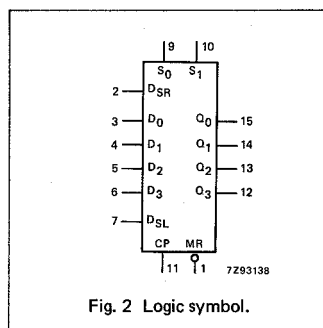
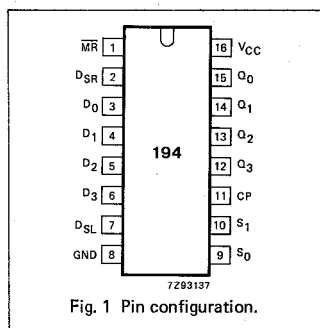
### PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).

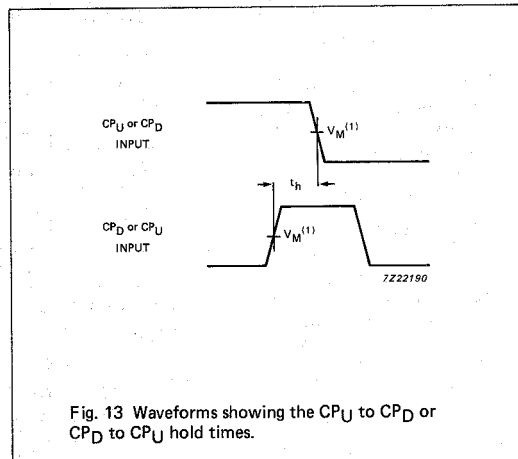
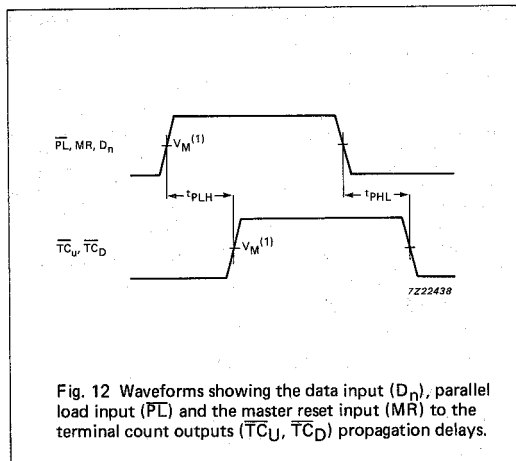
16-lead mini-pack; plastic (SO16; SOT109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	asynchronous master reset input (active LOW)
2	$D_{SR}$	serial data input (shift right)
3, 4, 5, 6	$D_0$ to $D_3$	parallel data inputs
7	$D_{SL}$	serial data input (shift left)
8	GND	ground (0 V)
9, 10	$S_0, S_1$	mode control inputs
11	CP	clock input (LOW-to-HIGH edge-triggered)
15, 14, 13, 12	$Q_0$ to $Q_3$	parallel outputs
16	$V_{CC}$	positive supply voltage



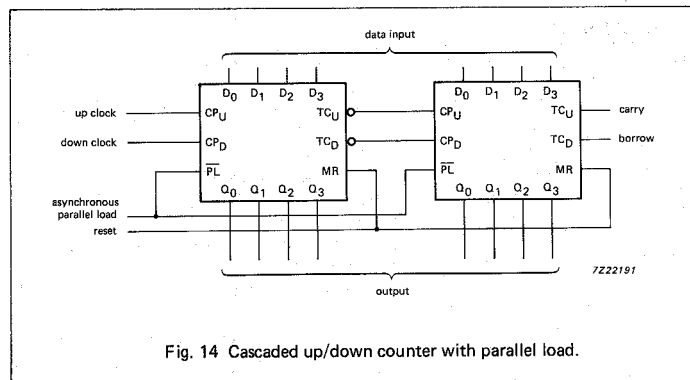
## AC WAVEFORMS (Cont'd)

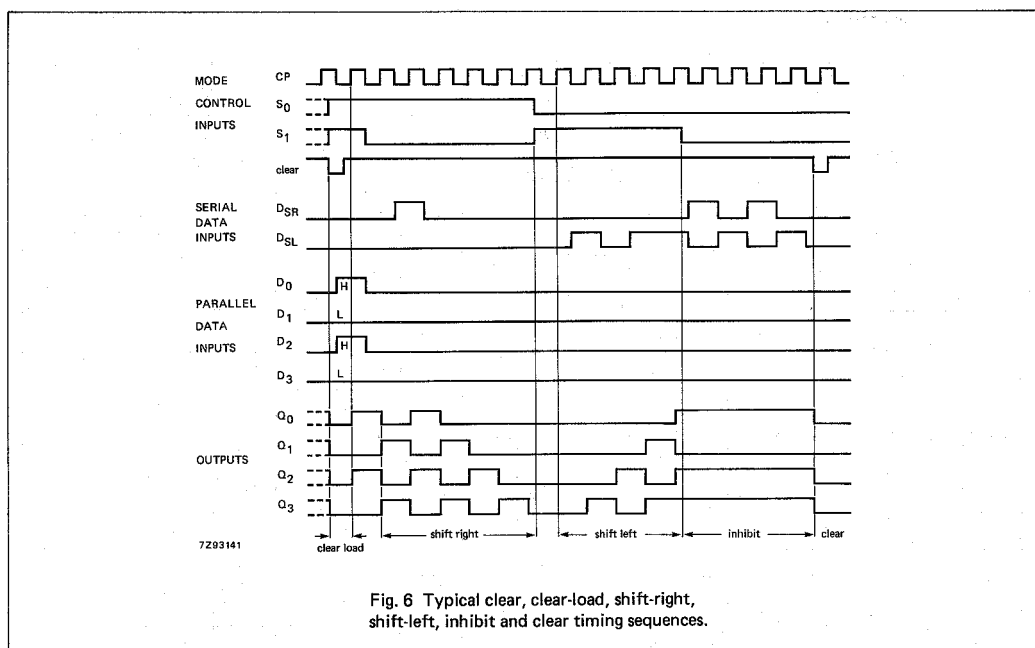


## Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

## APPLICATION INFORMATION



**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

74HC/HCT194  
MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HC									V <sub>CC</sub> V	WAVEFORMS
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 7	
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		39 14 11	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 8	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7	
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7	
t <sub>W</sub>	master reset pulse width: LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8	
t <sub>rem</sub>	removal time MR to CP	60 12 10	17 6 5		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8	
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	70 14 12	17 6 5		90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig. 9	
t <sub>su</sub>	set-up time S <sub>0</sub> , S <sub>1</sub> to CP	80 16 12	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10	
t <sub>su</sub>	set-up time DSR, DSL to CP	70 14 12	19 7 6		90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig. 9	
t <sub>h</sub>	hold time D <sub>n</sub> to CP	0 0 0	−14 −5 −4		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 9	
t <sub>h</sub>	hold time S <sub>0</sub> , S <sub>1</sub> to CP	0 0 0	−11 −4 −3		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 10	
t <sub>h</sub>	hold time DSR, DSL to CP	0 0 0	−17 −6 −5		0 0 0		0 0 0		ns	2.0 4.5 6.0		
f <sub>max</sub>	maximum clock pulse frequency	6.0 30 35	31 93 111		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 7	

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

$I_{CC}$  category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$D_n$	0.15
$D_{SR}, D_{SL}$	0.15
$CP$	0.50
$MR$	0.45
$S_n$	0.90