

# SN54ALS574B, SN54AS574, SN54AS575 SN74ALS574B, SN74ALS575A, SN74AS574, SN74AS575 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS165B – JUNE 1982 – REVISED JULY 1995

- 3-State Buffer-Type Noninverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Buffered Control Inputs
- SN74ALS575A and 'AS575 Have Synchronous Clear
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), Standard Plastic (N, NT) and Ceramic (J, JT) 300-mil DIPs, and Ceramic Flat (W) Packages

## description

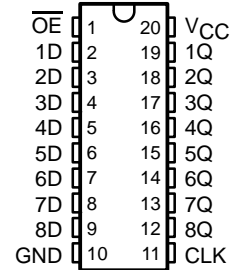
These octal D-type edge-triggered flip-flops feature 3-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops enter data on the low-to-high transition of the clock (CLK) input. The SN74ALS575A, SN54AS575, and SN74AS575 may be synchronously cleared by taking the clear (CLR) input low.

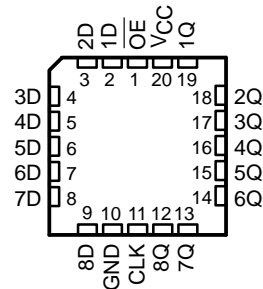
The output-enable ( $\overline{OE}$ ) input does not affect internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS574B, SN54AS574, and SN54AS575 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS574B, SN74ALS575A, SN74AS574, and SN74AS575 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

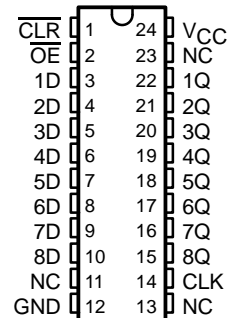
SN54ALS574B, SN54AS574 . . . J OR W PACKAGE  
SN74ALS574B, SN74AS574 . . . DW OR N PACKAGE  
(TOP VIEW)



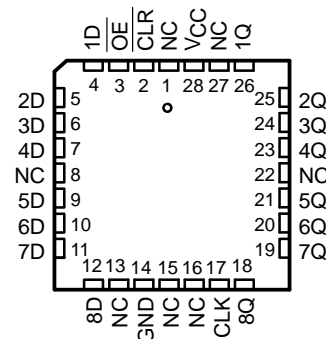
SN54ALS574B, SN54AS574 . . . FK PACKAGE  
(TOP VIEW)



SN54AS575 . . . JT OR W PACKAGE  
SN74ALS575A, SN74AS575 . . . DW OR NT PACKAGE  
(TOP VIEW)



SN54AS575 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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## Function Tables

SN54ALS574B, SN74ALS574B, SN54AS574, SN74AS574  
(each flip-flop)

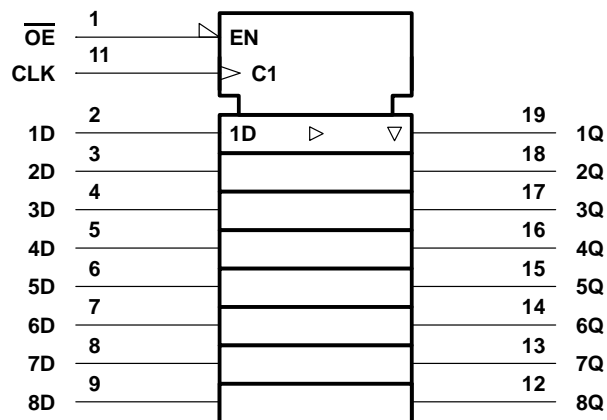
INPUTS			OUTPUT Q
$\overline{OE}$	CLK	D	
L	↑	H	H
L	↑	L	L
L	L	X	$Q_0$
H	X	X	Z

SN74ALS575A, SN54AS575, SN74AS575  
(each flip-flop)

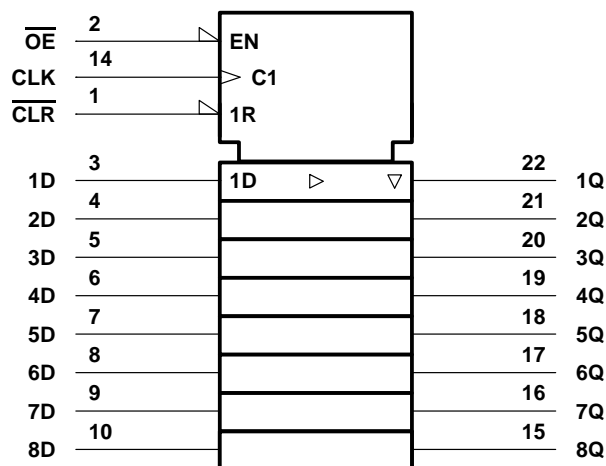
INPUTS				OUTPUT Q
$\overline{OE}$	CLR	CLK	D	
L	L	↑	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	$Q_0$
H	X	H	X	Z

## logic symbols†

SN54ALS574B, SN74ALS574B,  
SN54AS574, SN74AS574



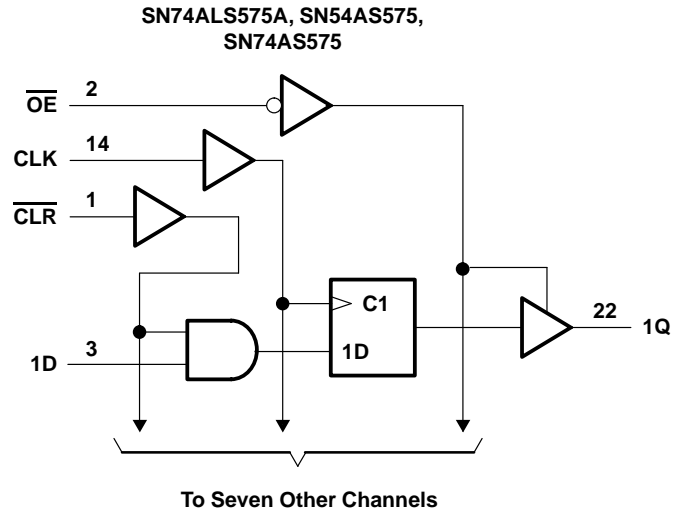
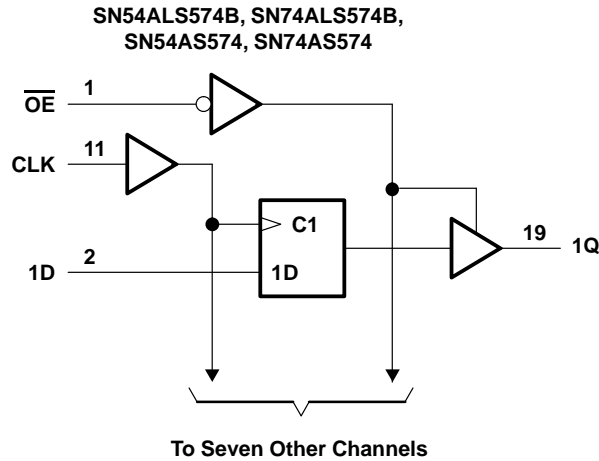
SN74ALS575A, SN54AS575,  
SN74AS575



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the DW, J, JT, N, and NT packages.

**SN54ALS574B, SN54AS574, SN54AS575**  
**SN74ALS574B, SN74ALS575A, SN74AS574, SN74AS575**  
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**logic diagrams (positive logic)**



Pin numbers shown are for the DW, J, JT, N, and NT packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, $T_A$ : SN54ALS574B	–55°C to 125°C
SN74ALS574B, SN74ALS575A	0°C to 70°C
Storage temperature range	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions**

		SN54ALS574B			SN74ALS574B SN74ALS575A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current			–1			–2.6	mA
$I_{OL}$	Low-level output current			12			24	mA
$f_{clock}$	Clock frequency	'ALS574B						MHz
		0		28	0		35	
$t_w$	Pulse duration	SN74ALS575A						ns
		16.5			14			
$t_{su}$	Setup time before CLK $\uparrow$	SN74ALS575A, CLK high or low						ns
		15			16.5			
$t_h$	Hold time after CLK $\uparrow$	Data						ns
		4			15			
$T_A$	Operating free-air temperature	SN74ALS575A, CLR						°C
		–55		125	0		70	

**SN54ALS574B, SN54AS574, SN54AS575**  
**SN74ALS574B, SN74ALS575A, SN74AS574, SN74AS575**  
**OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		SN54ALS574B			SN74ALS574B SN74ALS575A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = −18 mA		−1.2			−1.2			V
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = −0.4 mA		V <sub>CC</sub> − 2			V <sub>CC</sub> − 2			V
		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = −1 mA		2.4 3.3						
		I <sub>OH</sub> = −2.6 mA					2.4 3.2			
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 12 mA		0.25 0.4			0.25 0.4			V
		I <sub>OL</sub> = 24 mA					0.35 0.5			
I <sub>OZH</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V		20			20			μA
I <sub>OZL</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.4 V		−20			−20			μA
I <sub>I</sub>		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V		0.1			0.1			mA
I <sub>IH</sub>		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V		20			20			μA
I <sub>IL</sub>		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V		−0.2			−0.2			mA
I <sub>O†</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V		−20 −112			−30 −112			mA
I <sub>CC</sub>	‘ALS574B	V <sub>CC</sub> = 5.5 V	Outputs high	11 18		11 18		mA		
			Outputs low	17 27		17 27				
			Outputs disabled	17 28		17 28				
	SN74ALS575A	V <sub>CC</sub> = 5.5 V	Outputs high	10 17		10 17				
			Outputs low	15 24		15 24				
			Outputs disabled	16 30		16 30				

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC = 4.5 V to 5.5 V, CL = 50 pF, R1 = 500 Ω, R2 = 500 Ω, TA = MIN to MAX§						UNIT
			SN54ALS574B		SN74ALS574B		SN74ALS575A		
			MIN	MAX	MIN	MAX	MIN	MAX	
fmax			28		35		30		MHz
tPLH	CLK	Q	4	22	3	14	4	14	ns
tPHL			4	17	4	14	4	14	
tPZH	OE	Q	4	21	3	18	4	18	ns
tPZL			4	26	4	18	4	18	
tPHZ	OE	Q	2	16	1	10	2	10	ns
tPLZ			2	25	2	12	3	13	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



**SN54ALS574B, SN54AS574, SN54AS575**  
**SN74ALS574B, SN74ALS575A, SN74AS574, SN74AS575**  
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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, $T_A$ : SN54AS574, SN54AS575	–55°C to 125°C
SN74AS574, SN74AS575	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions**

			SN54AS574 SN54AS575			SN74AS574 SN74AS575			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage		2			2			V
V <sub>IL</sub>	Low-level input voltage				0.8			0.8	V
I <sub>OH</sub>	High-level output current				−12			−15	mA
I <sub>OL</sub>	Low-level output current				32			48	mA
f <sub>clock</sub> *	Clock frequency		0		100	0		90	MHz
t <sub>w</sub> *	Pulse duration	CLK high	5			5.5			ns
		CLK low	4			5.5			
t <sub>su</sub> *	Setup time before CLK↑	Data	3			5.5			ns
		‘AS575, $\overline{\text{CLR}}$ high or low	6.5			6.5			
t <sub>h</sub> *	Hold time after CLK↑	Data	3			3			ns
		‘AS575, $\overline{\text{CLR}}$	0			0			
T <sub>A</sub>	Operating free-air temperature		−55		125	0		70	°C

\* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.



**SN54ALS574B, SN54AS574, SN54AS575**  
**SN74ALS574B, SN74ALS575A, SN74AS574, SN74AS575**  
**OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		SN54AS574 SN54AS575		SN74AS574 SN74AS575		UNIT		
				MIN	TYP†	MAX	MIN		TYP†	MAX
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = −18 mA		−1.2		−1.2		V		
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = −2 mA		V <sub>CC</sub> − 2		V <sub>CC</sub> − 2		V		
		V <sub>CC</sub> = 4.5 V I <sub>OH</sub> = −12 mA		2.4	3.2					
		I <sub>OH</sub> = −15 mA				2.4	3.3			
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V I <sub>OL</sub> = 32 mA		0.29	0.5			V		
		I <sub>OL</sub> = 48 mA				0.34	0.5			
I <sub>OZH</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V		50		50		μA		
I <sub>OZL</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.4 V		−50		−50		μA		
I <sub>I</sub>		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V		0.1		0.1		mA		
I <sub>IH</sub>		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V		20		20		μA		
I <sub>IL</sub>	OE, CLK, CLR	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V		−0.5		−0.5		mA		
	D			−3		−2				
I <sub>O†</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V		−30	−112	−30	−112	mA		
I <sub>CC</sub>	'AS574	V <sub>CC</sub> = 5.5 V		Outputs high		73	116	73	116	mA
				Outputs low		85	134	85	134	
				Outputs disabled		84	134	84	134	
	'AS575	V <sub>CC</sub> = 5.5 V		Outputs high		78	126	78	126	
				Outputs low		89	142	89	142	
				Outputs disabled		88	142	88	142	

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX§				UNIT
			SN54AS574 SN54AS575		SN74AS574 SN74AS575		
			MIN	MAX	MIN	MAX	
f <sub>max</sub> *			100		90		MHz
t <sub>PLH</sub>	CLK	Any Q	3	11	3	8	ns
t <sub>PHL</sub>			4	11	4	9	
t <sub>PZH</sub>	OE	Any Q	2	7	2	6	ns
t <sub>PZL</sub>			3	11	3	10	
t <sub>PHZ</sub>	OE	Any Q	2	7	2	6	ns
t <sub>PLZ</sub>			2	7	2	6	

\* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

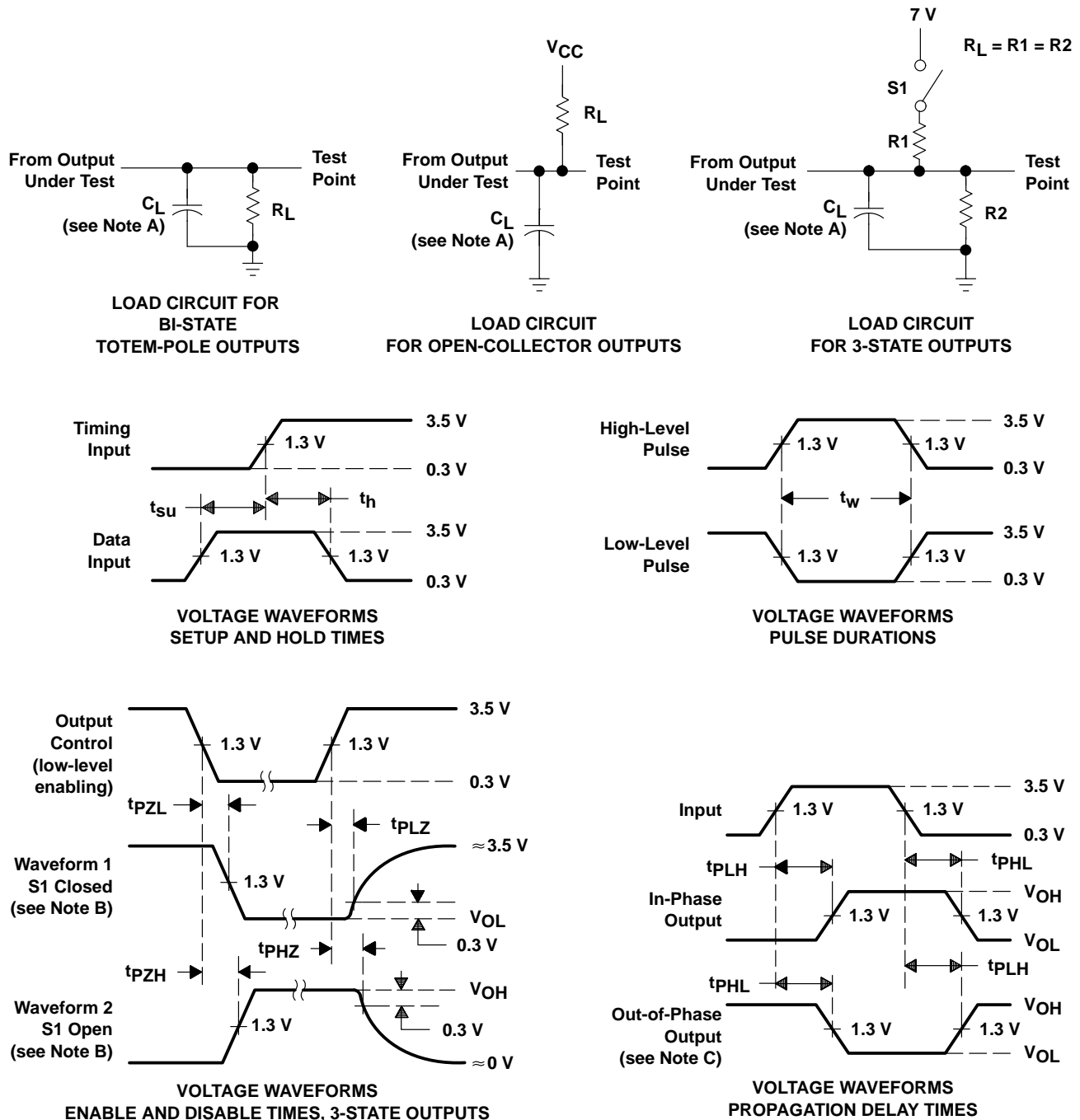
\S For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



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SN74ALS574B, SN74ALS575A, SN74AS574, SN74AS575  
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**PARAMETER MEASUREMENT INFORMATION  
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

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