

## CD4030M/CD4030C Quad EXCLUSIVE-OR Gate

### General Description

The EXCLUSIVE-OR gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. All inputs are protected against static discharge with diodes to  $V_{DD}$  and  $V_{SS}$ .

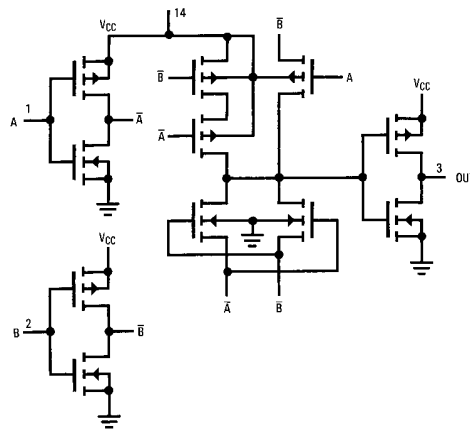
### Features

- Wide supply voltage range 3.0V to 15V
- Low power 100 nW (typ.)
- Medium speed operation  $t_{PHL} = t_{PLH} = 40$  ns (typ.)  
at  $C_L = 15$  pF, 10V supply
- High noise immunity 0.45  $V_{CC}$  (typ.)

### Applications

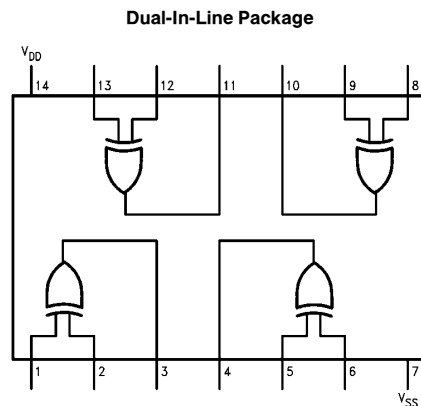
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Industrial controls
- Remote metering
- Computers

### Schematic Diagram



TL/F/5961-1

### Connection Diagram



TL/F/5961-2

Order Number CD4030

## Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin (Note 1)  $V_{SS} - 0.3V$  to  $V_{SS} + 15.5V$

Operating Temperature Range

CD4030M

CD4030C

−55°C to +125°C

−40°C to +85°C

Storage Temperature Range

−65°C to +150°C

Power Dissipation ( $P_D$ )

Dual-In-Line

700 mW

Small Outline

500 mW

Operating  $V_{DD}$  Range

$V_{SS} + 3.0V$  to  $V_{SS} + 15V$

Lead Temperature

(Soldering, 10 seconds)

260°C

## DC Electrical Characteristics CD4030M

Symbol	Parameter	Conditions	Limits									Units
			−55°C			+25°C			+125°C			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I <sub>L</sub>	Quiescent Device Current	V <sub>DD</sub> = 5.0V V <sub>DD</sub> = 10V			0.5 1.0		0.005 0.01	0.5 1.0			30 60	μA μA
P <sub>D</sub>	Quiescent Device Dissipation Package	V <sub>DD</sub> = 5.0V V <sub>DD</sub> = 10V			2.5 10		0.025 0.1	2.5 10			150 600	μW μW
V <sub>OL</sub>	Output Voltage Low Level	V <sub>DD</sub> = 5.0V V <sub>DD</sub> = 10V			0.05 0.05		0 0	0.05 0.05			0.05 0.05	V V
V <sub>OH</sub>	Output Voltage High Level	V <sub>DD</sub> = 5.0V V <sub>DD</sub> = 10V	4.95 9.95			4.95 9.95	5.0 10		4.95 9.95			V V
V <sub>NL</sub>	Noise Immunity (All Inputs)	V <sub>DD</sub> = 5.0V V <sub>DD</sub> = 10V	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V V
V <sub>NH</sub>	Noise Immunity (All Inputs)	V <sub>DD</sub> = 5.0V V <sub>DD</sub> = 10V	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V V
I <sub>DN</sub>	Output Drive Current N-Channel (Note 2)	V <sub>DD</sub> = 5.0V V <sub>DD</sub> = 10V	0.75 1.5			0.6 1.2	1.2 2.4		0.45 0.9			mA mA
I <sub>DP</sub>	Output Drive Current P-Channel (Note 2)	V <sub>DD</sub> = 5.0V V <sub>DD</sub> = 10V	−0.45 −0.95			−0.3 −0.65	−0.6 −1.3		−0.21 −0.45			mA mA
I <sub>I</sub>	Input Current	V <sub>I</sub> = 0V or V <sub>I</sub> = V <sub>DD</sub>					10					pA

## DC Electrical Characteristics CD4030C

Symbol	Parameter	Conditions	Limits									Units
			− 40°C			+ 25°C			+ 85°C			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I <sub>L</sub>	Quiescent Device Current	V <sub>DD</sub> = 5.0V V <sub>DD</sub> = 10V			5.0 10		0.05 0.1	5.0 10			70 140	μA μA
P <sub>D</sub>	Quiescent Device Dissipation Package	V <sub>DD</sub> = 5.0V V <sub>DD</sub> = 10V			25 100		0.25 1.0	25 100			350 1,400	μW μW
V <sub>OL</sub>	Output Voltage Low Level	V <sub>DD</sub> = 5.0V V <sub>DD</sub> = 10V			0.05 0.05		0 0	0.05 0.05			0.05 0.05	V V
V <sub>OH</sub>	Output Voltage High Level	V <sub>DD</sub> = 5.0V V <sub>DD</sub> = 10V	4.95 9.95			4.95 9.95	5.0 10		4.95 9.95			V V
V <sub>NL</sub>	Noise Immunity (All Inputs)	V <sub>DD</sub> = 5.0V V <sub>DD</sub> = 10V	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V V
V <sub>NH</sub>	Noise Immunity (All Inputs)	V <sub>DD</sub> = 5.0V V <sub>DD</sub> = 10V	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V V
I <sub>DN</sub>	Output Drive Current N-Channel (Note 2)	V <sub>DD</sub> = 5.0V V <sub>DD</sub> = 10V	0.35 0.7			0.3 0.6	1.2 2.4		0.25 0.5			mA mA
I <sub>DP</sub>	Output Drive Current P-Channel (Note 2)	V <sub>DD</sub> = 5.0V V <sub>DD</sub> = 10 V	−0.21 −0.45			−0.15 −0.32	−0.6 −1.3		−0.12 −0.25			mA mA
I <sub>I</sub>	Input Current	V <sub>I</sub> = 0V or V <sub>I</sub> = V <sub>DD</sub>					10					pA

## AC Electrical Characteristics\* CD4030M

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
$t_{PHL}$	Propagation Delay Time	$V_{DD} = 5.0V$ $V_{DD} = 10V$		100	200	ns
				40	100	ns
$t_{PLH}$	Propagation Delay Time	$V_{DD} = 5.0V$ $V_{DD} = 10V$		100	200	ns
				40	100	ns
$t_{THL}$	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		70	150	ns
				25	75	ns
$t_{TLH}$	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		80	150	ns
				30	75	ns
$C_I$	Input Capacitance	$V_I = 0V$ or $V_I = V_{DD}$		5.0		pF

\*AC Parameters are guaranteed by DC correlated testing.

## AC Electrical Characteristics\* CD4030C

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
$t_{PHL}$	Propagation Delay Time	$V_{DD} = 5.0V$ $V_{DD} = 10V$		100	300	ns
				40	150	ns
$t_{PLH}$	Propagation Delay Time	$V_{DD} = 5.0V$ $V_{DD} = 10V$		100	300	ns
				40	150	ns
$t_{THL}$	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		70	300	ns
				25	150	ns
$t_{TLH}$	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		80	300	ns
				30	150	ns
$C_I$	Input Capacitance	$V_I = 0V$ or $V_I = V_{DD}$		5.0		pF

\*AC Parameters are guaranteed by DC correlated testing.

**Note 1:** This device should not be connected to circuits with power on because high transient voltages may cause permanent damage.

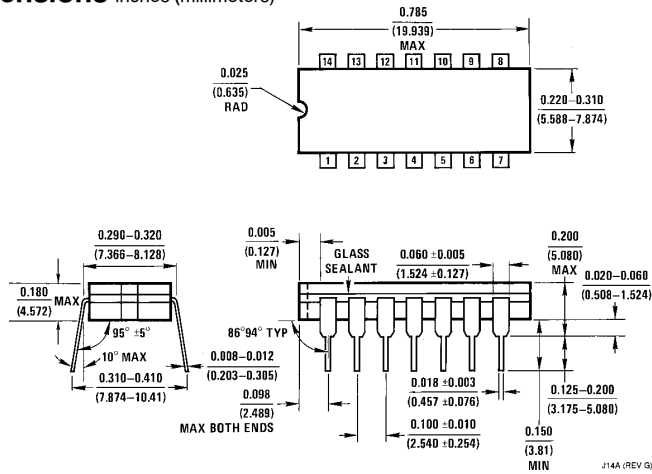
**Note 2:**  $I_{DN}$  and  $I_{DP}$  are tested one output at a time.

## Truth Table (For One of Four Identical Gates)

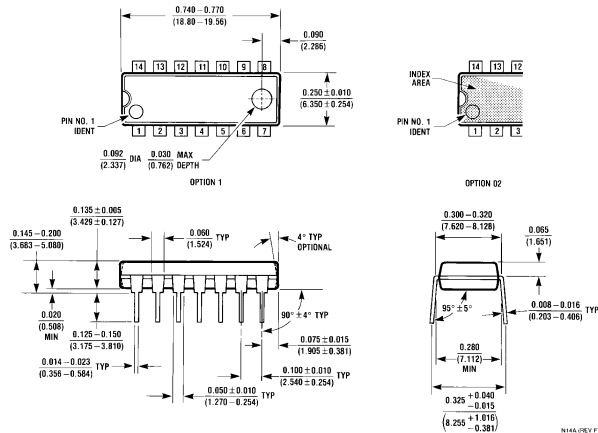
A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

Where: "1" = High Level  
"0" = Low Level

## Physical Dimensions inches (millimeters)



**Ceramic Dual-In-Line Package (J)**  
**Order Number CD4030MJ or CD4030CJ**  
**NS Package Number J14A**



**Molded Dual-In-Line Package (N)**  
**Order Number CD4030MN or CD4030CN**  
**NS Package Number N14A**

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